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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,503	04/01/2004	Hong-Jyh Li	2004P51130US/I331.128.101	8623

7590 07/10/2006

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EXAMINER	
JOHNSTON, PHILLIP A	

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 07/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,503	LI, HONG-JYH	
	Examiner	Art Unit	
	Phillip A. Johnston	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This Office Action is submitted in response to the RCE/Amendment filed 5-17-2006, wherein claims 4,8,10,11,14,16,17,20,23, and 28-31 have been amended. Claims 1-31 are pending.

Claims Rejection – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. No. 2004/0107909 to Collins, in view of King, U.S. Patent No. 6,855,994.

Collins (909) discloses the following;

(a) A plasma immersion ion implantation apparatus that includes vacuum chamber 8010, pump 8035, wafer holder 8025, gas supply 8045, and plasma generator power source 8055, 8050, and 8051, as recited in claims 1,6-8,16, and 25. See paragraphs [0249] - [0251]; and Figure 79 below;

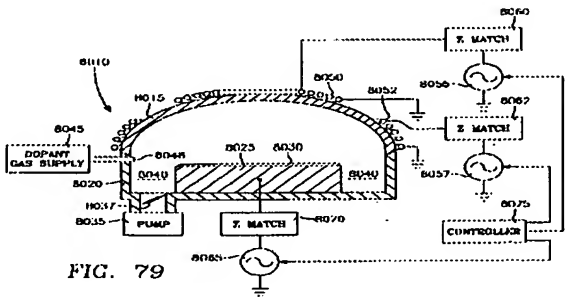

FIG. 79

(b) The use of N, B, As, and Sb ions, as recited in claims 2,3,10,11,26, and 27. See paragraph [0249];

(c) A plasma source with current alternating at RF frequency equivalent to the AC voltage source recited in claims 5,24, and 29. See paragraph [0126];

(d) An apparatus and method of fabricating a MOSFET having a high-k SiO_2 dielectric layer 9962, doped with Nitrogen (N) ions via implantation, as recited in claims 1,8,12,16-19, and 25. See paragraphs [0310]; [0321];

Collins (909) as applied above fails to teach the use of a high-k dielectric layer having a k-value greater than 9, as recited in amended claims 1,8,16, and 25. However, King (994) discloses an embodiment that includes the deposition of a high dielectric constant layer at the silicon substrate surface prior to the deposition of the polysilicon gate 18. A suitable high dielectric constant layer can be a silicon nitride, zirconium oxide, or hafnium silicate (HfSiO). Thereafter, oxygen implantation into the silicon substrate and/or polysilicon gate followed by annealing, as in the process of FIGS. 1D-1F, will grow a very thin (≤ 2 run) silicon oxide with well-controlled thickness. The thin silicon oxide can serve as the buffer layer or interfacial layer that is critical to the attainment of high carrier mobility and low interface defects, as recited in claims 1,8,16, and 25. See Column 4, line 26-40; and Figures 1D and1E below.

King (994) also discloses a dose range from 10^{15} to 10^{16} ions/cm^2, as recited in claim 30. See Column 1, line 65-67; and Column 2, line 1-18.

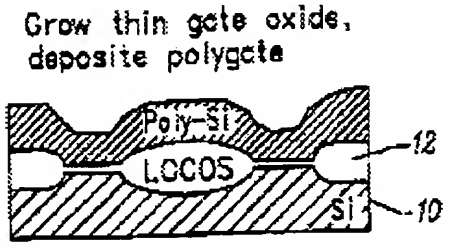

FIG. 1D

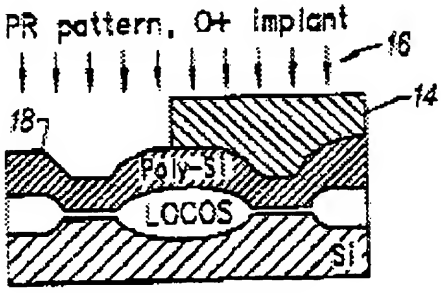

FIG. 1E

Therefore it would have been obvious to one of ordinary skill in the art that the ion implantation apparatus and method of Collins (909) can be modified to use the implant method of King (994), to provide an oxygen-implanted oxide layer under a high dielectric constant layer under a polysilicon gate, , thereby providing an improved multiple-thickness gate oxide for transistors on a single semiconductor die.

4. Claims 4,8,10,11,14,16,17,20,23,25,28,30, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins (909) and King (994) in view of Chan, U.S. Patent No. 5,449,920.

The combination of Collins (909) and King (994) fails to teach an ion implantation apparatus having;

(a) A constant DC voltage source, as recited in claims 4,8,23, and 28;

(b) Acceleration of positive ions, as recited in claims 8,10,11,14,16,17,20,25, and 30; and

(c) Ion energies, as recited in claim 31.

However, Chan (920) discloses a wafer holder 110 or 110' connected to a negative constant DC or pulsed bias voltage source 122 which biases the wafer 115 to a predefined negative potential, and a grid 286 that, acts as a shutter, where positive ions see the negative potential on the wafer holder and are accelerated. A bias voltage (ion energy) of between 1-100 kV is normally applied. See Column 5, line 60-68; Column 6, line 1-3; Figure 3; and Figure 5 below.

Therefore it would have been obvious to one of ordinary skill in the art that the ion implantation apparatus and method of Collins (909) and King (994) can be modified to use the constant voltage apparatus and method of Chan (920), to provide a constant DC voltage source and expose the substrate only to ions having prescribed characteristics to provide a uniform implantation layer.

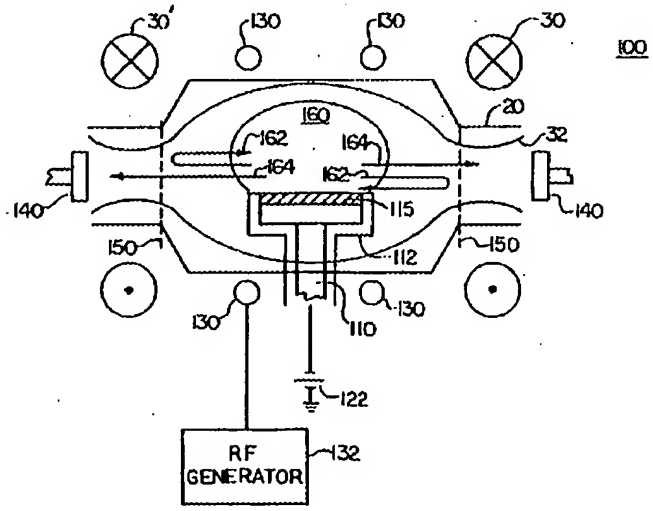

FIG. 3

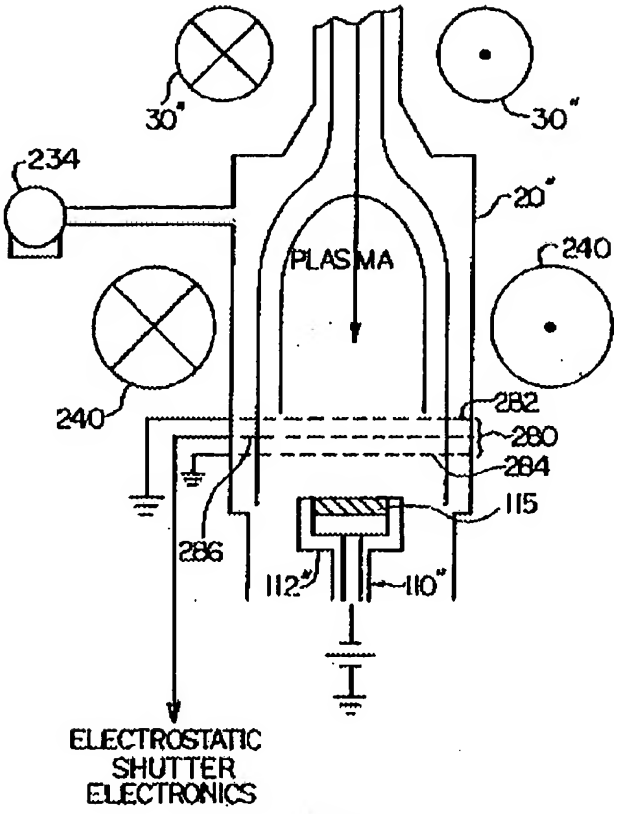

FIG. 5

Conclusion

5. Any inquiry concerning this communication or earlier communications should be directed to Phillip Johnston whose telephone number is (571) 272-2475. The examiner can normally be reached on Monday-Friday from 6:30 am to 3:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor John Lee can be reached at (571) 272-2477. The fax phone number for the organization where the application or proceeding is assigned is 571 273 8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PJ

June 29, 2006

Nikita Wells

NIKITA WELLS
PRIMARY EXAMINER 06/30/06